KAF Series Full-Frame CCD Sensors

Binning Mode Operation

(9mm Pixel KAF Image Sensors)

Eastman Kodak Company
Microelectronics Technology Division

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1.0 Binning Recommendations

Recommended CCD settings for operating Eastman Kodak's 9µm pixel Full Frame CCD sensors in binning applications are shown below. Bold type indicates possible deviation from the nominal setting in the Device Performance Specifications.

DC Operating Conditions

VRD	**11.5V**
VSS	2.0 V
VDD	15.0V
VSUB	0.0V
VOG	**3.0V**
LOD/GAURD	9.0V

AC Operating Conditions

V1 Clock High	0.5V
V1 Clock Low	-9.0V
V2 Clock High	0.5 V
V2 Clock Low	-9.0 V
H1 Clock High	6.0V
H1 Clock Low	-4.0V
H2 Clock High	6.0V
H2 Clock Low	-4.0 V
Reset clock High	4.0V
Reset clock Low	**-3.0V**

Performance Specifications

Output Amplifier Sensitivity	10uV/e	
Vertical CCD Capacity	1.2V	(120,000 electrons)
Horizontal CCD Capacity	2.4V	(240,000 electrons)
Output Node Capacity	**3.3V**	**(330,000 electrons)**

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2.0 Introduction

This Application note is intended to describe how to operate Eastman Kodak's 9µm Pixel Full Frame CCD sensors for binning applications. It also deals with the performance issues that should be considered.

The applicable CCD sensors include:

KAF 040X (0400, 0400L, 0401)
KAF 160X (1600, 1601, 1602 ...)
KAF 420X (4200, 4201, ...)
KAF 630X (6300, 6301 ...)
KAF 16800

3.0 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the CCD sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength.

4.0 Charge Transport: Normal Mode (See Figure 1.)

After the CCD has been illuminated, the charge accumulated in the pixel sites is clocked out of the sensor in a two step process. When operating in a normal, or non-binning, mode, a single line (row) of charge is first shifted out of the vertical CCD array and into the horizontal CCD register in parallel. The line of charge is then serially shifted to the floating diffusion output node, pixel by pixel. Each pixel's charge is converted into a voltage and is sensed off chip. After the CCD output signal has been sampled by the system electronics, the charge on the floating diffusion is removed via the Reset Drain by action of the Reset Clock. The floating diffusion is reset to the potential applied by VRD. This is repeated for all succeeding pixels in the line, and lines in the array.

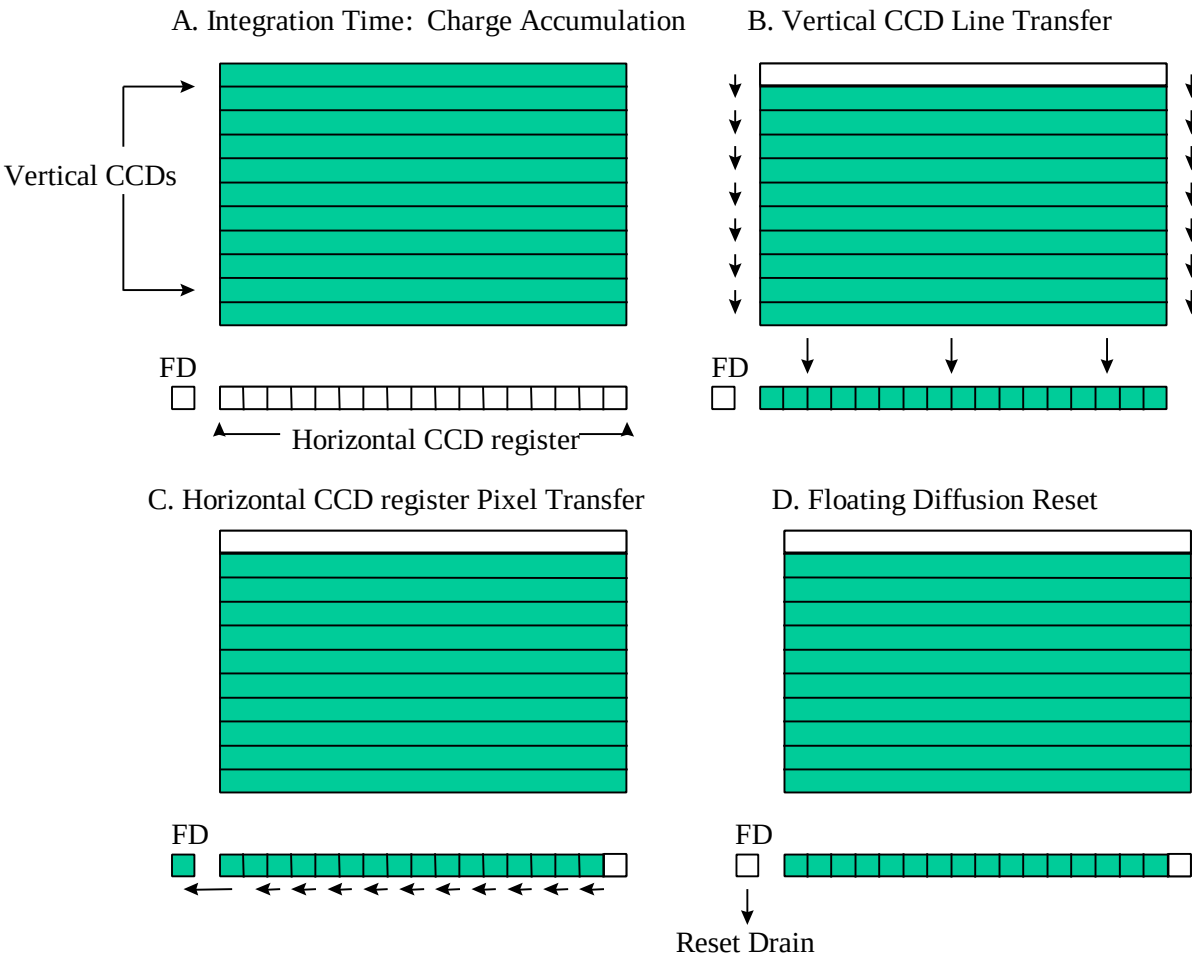

Figure 1 Charge Transport: Normal Mode

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5.0 Charge Transport: Binning Mode

When operating the CCD sensor in a binning mode, two or more lines of charge are shifted into the horizontal CCD register in parallel, before the horizontal clocks begin to shift the charge towards the floating diffusion output node. This charge is then serially shifted to the output, pixel by pixel, the same as in normal mode. However, several horizontal CCD's worth of charge (usually the same number as the lines that were transferred in from the vertical CCD array before horizontal clocking) are allowed to accumulate on the floating diffusion node before being sensed off chip and removed by the Reset Clock.

Example: A CCD is being operated in a 2x2 binning mode. (See Figure 2.)

The charge in line 1's pixels is shifted into the horizontal CCD.
The charge in line 2's pixels is then shifted into the horizontal CCD.

The accumulated charge in the horizontal register is now: (line1 + line 2).

The first pixel in the horizontal CCD is shifted to the output diffusion node.
The second pixel in the horizontal CCD is shifted to the output diffusion node.

The accumulated charge on the output diffusion node is now:
(line1,pix1)+(line2, pix1)+(line1, pix2)+(line2, pix2)

This is the total accumulated charge of the 2x2 block of pixels.

The reset clock now removes the accumulated charge after being sensed off chip.

The next 2 pixels are shifted out of the horizontal CCD and onto the floating diffusion node. This accumulated charge (the next 2x2 block) is removed by the reset clock after being sensed off chip. And so on ...

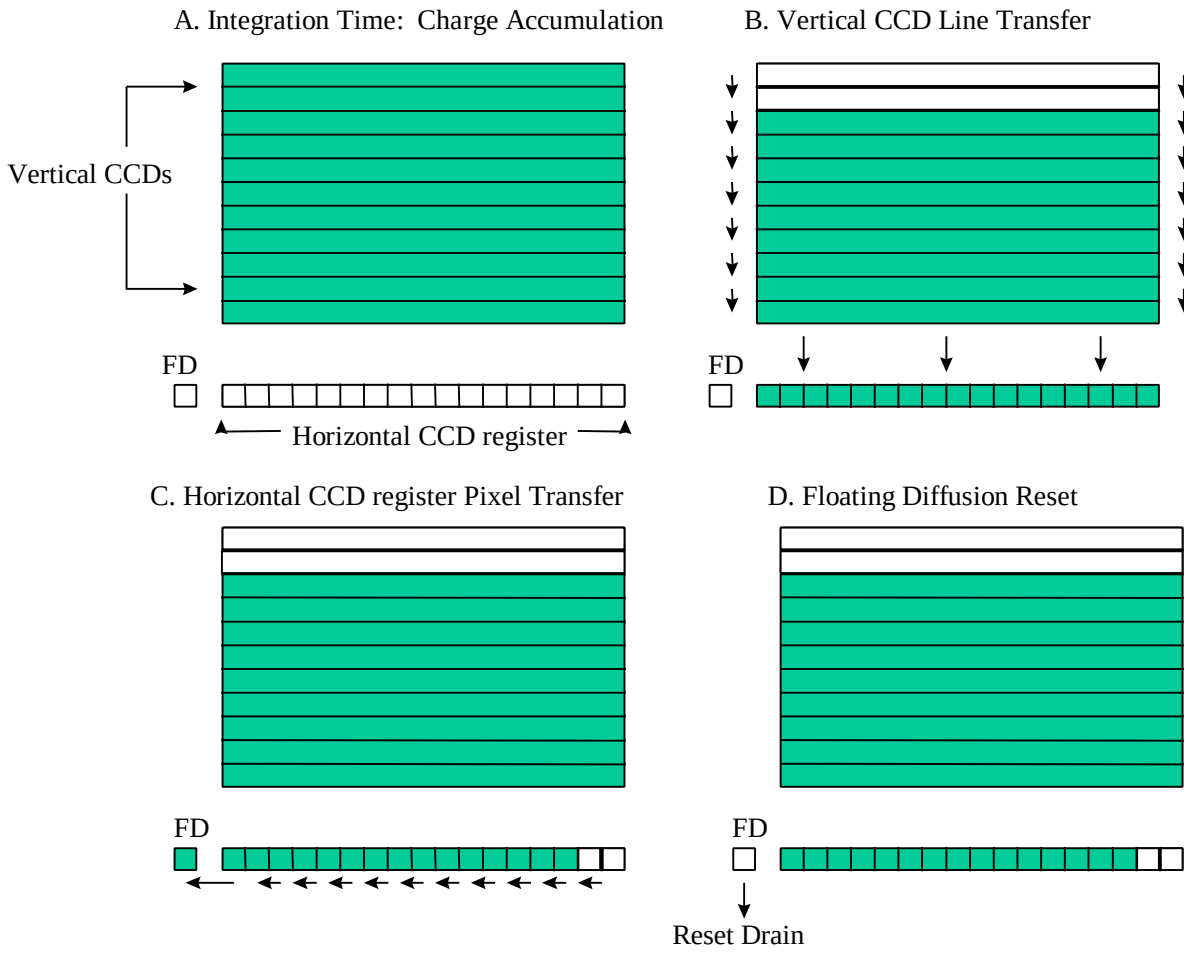

Figure 2 Charge Transport: 2X2 Binning Mode

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6.0 Binning Timing

To operate a CCD in binning mode, adjustments must be made to the CCD clocks timing, as well as the video processing signals timing.

6.1 Vertical Clocks:

The Vertical Clocks (V1, V2) shift lines of charge into the horizontal CCD register in parallel, while H1 is held high and H2 is held low.

Clocking the Full Frame Sensor in the sequence shown in Figure 3 parallel shifts the accumulated charge in the Vertical CCD's over one line. On the rising edge of V2, the line of charge in the last Vertical CCD line is transported into the Horizontal CCD register.

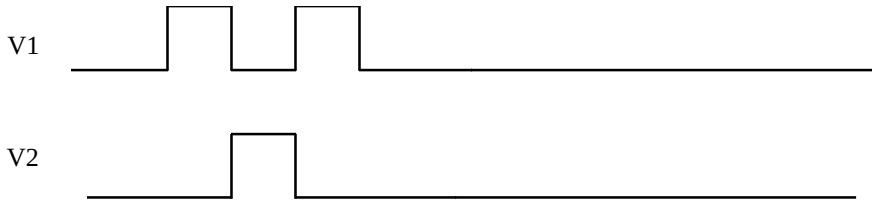


Figure 3 Vertical Timing: Normal mode

When operating the CCD in a binning mode, an additional sequence of the V1 and V2 clocks is repeated as many times as the binning mode dictates before beginning to clock the charge out of the horizontal CCD register. In the 2x2 binning mode example the clocks would look like Figure 4. Two lines of charge would be transported onto the Horizontal CCD register.

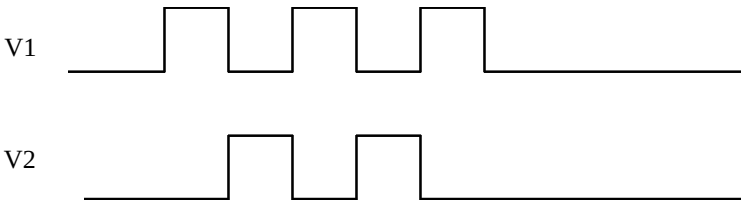


Figure 4 Vertical Timing: 2X2 Binning Mode

6.2 Horizontal Clocks:

The Horizontal Clocks (H1, H2) serially shift lines of charge to the output, pixel by pixel. These horizontal clocks are run the same regardless of whether or not the CCD is operating in binning mode or not.

6.3 Reset Clock:

The Reset clock removes the charge from the floating diffusion node and resets the floating diffusion potential to the VRD bias. When operating the CCD in normal mode (no binning) this is done every pixel after the charge has been sensed off chip. (See Figure 5.)

Figure 5 Reset Clocking in Normal Mode

When operating the CCD in a binning mode, the frequency of the Reset clock is decreased depending on the operating binning mode to allow the charge from two or more pixels to accumulate on the floating diffusion output node before being sensed off chip and removed via the reset drain. In the 2x2 binning mode example the Reset clock would look like Figure 6.

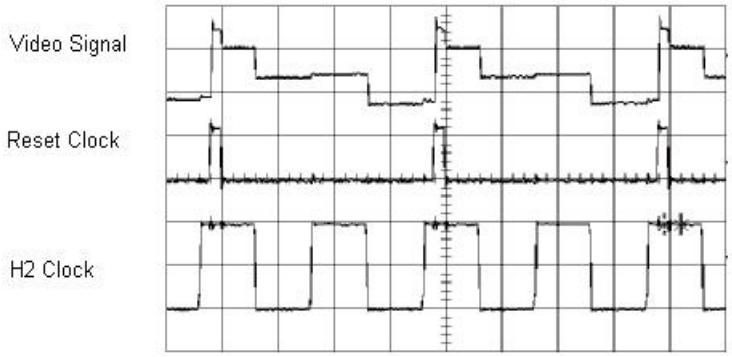


Figure 6 Reset clocking in 2x2 binning Mode

6.4 Correlated Double Sampling (CDS)

The CCD output video signal is measured at two points to determine the signal level of a particular pixel. The Clamp signal is synced to the video signal's reference level, and the Sample signal is synced to the video signal at the point after the charge has been shifted onto the floating diffusion node. The actual signal level for the pixel is the difference between the measurements taken at these two points.

Therefore the Clamp and Sample pulses have to be synchronized to the video signal so that these measurements are taken at the proper time.

When operating the CCD in a binning mode the frequency of the Clamp and Sample signals is decreased by the same amount as the Reset clock. See Figure 7 for a 2x2 binning example of the CDS signals and their relationship to the video signal, as well as to the Reset clock.

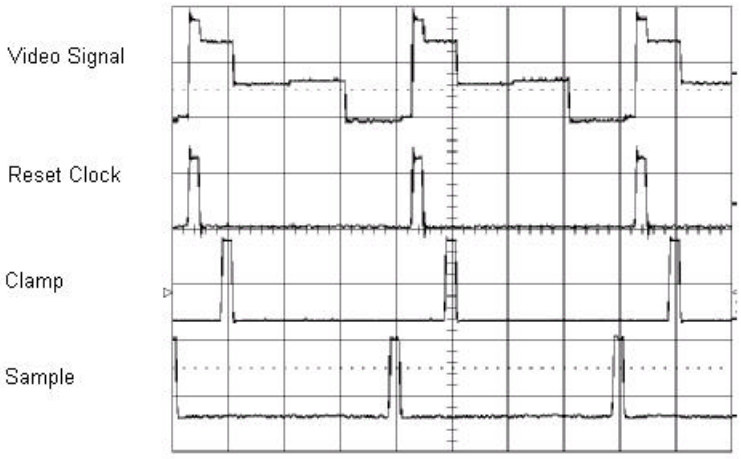


Figure 7 CDS Timing in 2X2 Binning Mode

7.0 Pixel Saturation: Nominal CCD settings

Nominal CCD settings refer to the CCD clock swings and CCD bias voltages as recommended in the Device specification sheet.

7.1 Non Binning Operation

When operating a 9 µm Pixel KAF-Series CCD with the nominal settings as dictated in the Device Specifications Sheet, the Floating Diffusion charge capacity is about the same as the Horizontal CCD charge capacity which is twice as large as the Vertical CCD charge capacity.

Vertical CCD charge capacity	=	100000 - 120000 electrons
Horizontal CCD charge capacity	=	200000 - 240000 electrons
Floating diffusion charge capacity	=	220000 - 240000 electrons

When operating the CCD in a non-binning mode, a pixel will saturate if the vertical CCD's charge capacity is exceeded.

7.2 Binning Operation

When operating the CCD in a binning mode, there are two additional factors that must be considered when determining when a pixel will saturate, the Horizontal CCD's charge capacity and the Floating Diffusion charge capacity.

A binned pixel will saturate if the sum of the electrons transported from the vertical CCD's into the horizontal register exceeds the Horizontal CCD charge capacity.

A binned pixel will also saturate if the sum of the electrons transported from the Horizontal CCD's onto the Floating Diffusion exceeds the Floating Diffusion charge capacity.

Figure 8 shows the Floating Diffusion charge capacity just before saturation with the sensor being operated in 2X2 Binning mode at the performance specifications nominal values.

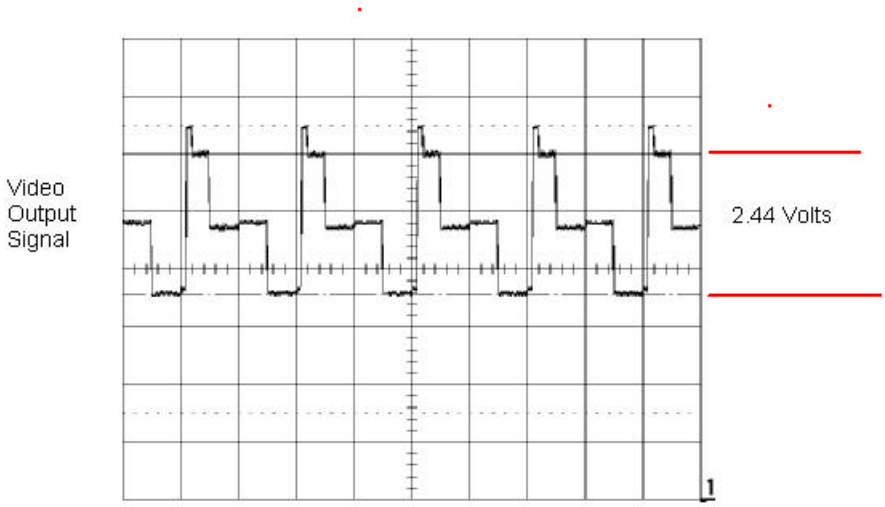


Figure 8 Floating Diffusion Charge Capacity (Nominal Settings)

8.0 Pixel Saturation: Adjusted CCD settings

The floating diffusion output node capacity depends on several variables, namely VRD, VOG and the Reset clock. At the nominal settings suggested in the CCD performance specifications, the output node capacity, Qtot, is about the same as the Horizontal CCD capacity.

In order to increase the charge capacity, Qtot, of the floating diffusion output node, the floating diffusion well depth must be increased. This is achieved by making VOG less positive and making VRD more positive. The low level of the Reset clock must also be made less positive.

By adjusting VRD more positive to 11.5 volts and VOG less positive to 3 volts, as well as adjusting the low level of the Reset clock voltage swing to -3 volts, the Floating Diffusion charge capacity can be increased to about 330000 electrons.

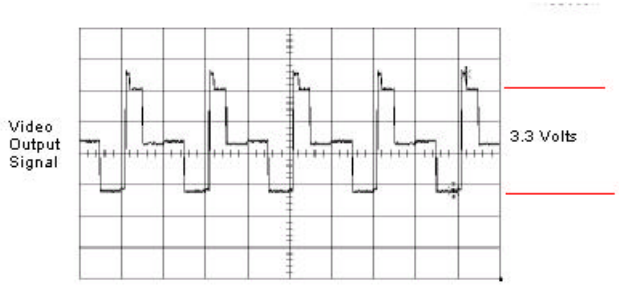


Figure 9 Floating Diffusion Capacity after VRD, VOG, Reset Adjustments

9.0 Saturated Video Output Signal

Charge is dumped onto the Floating Diffusion (FD) on the falling edge of H2. If enough electrons are present, they can flow back over the output gate if VOG is set too positive. Figure 11 illustrates the effect this has on the video output.

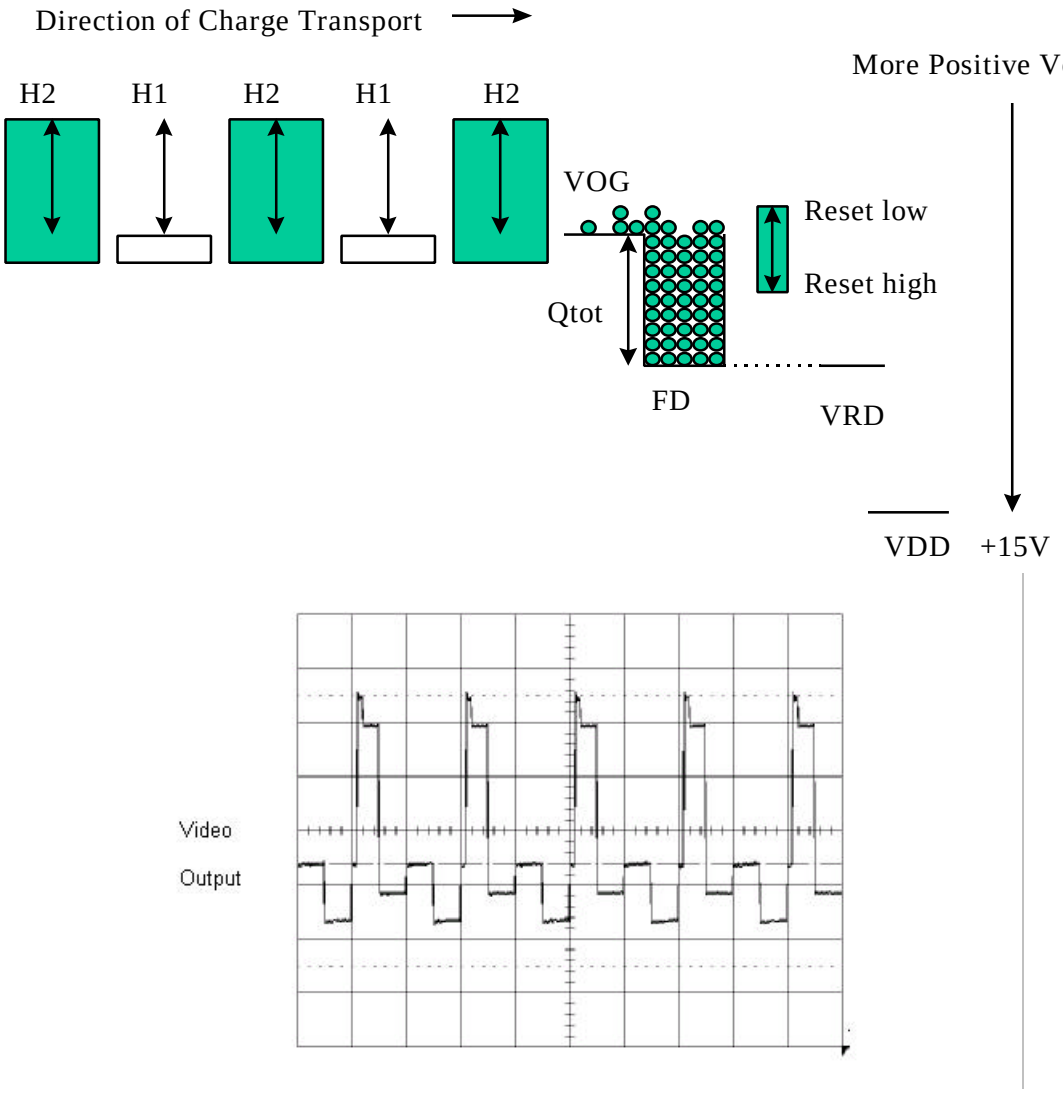
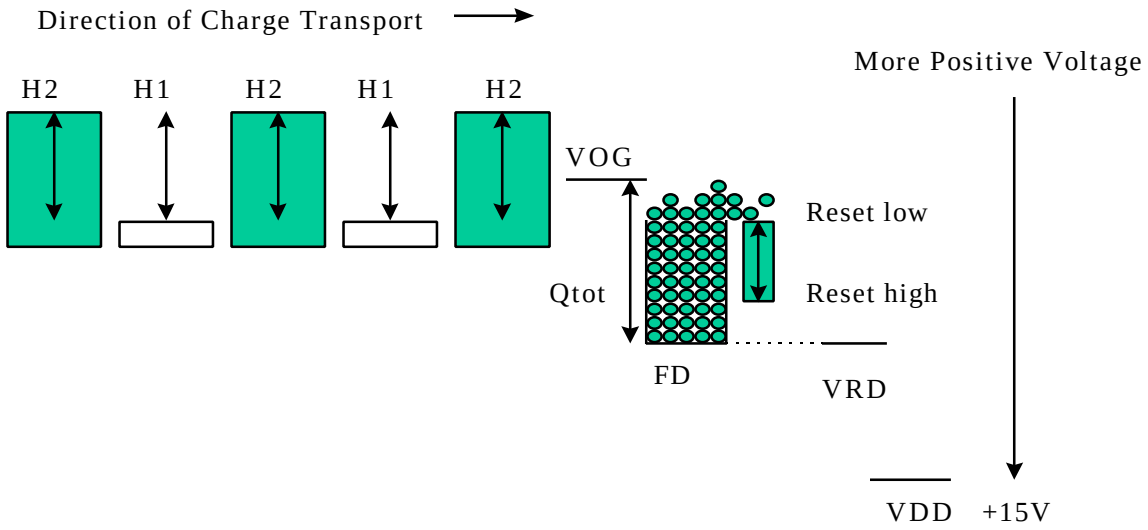


Figure 10 Charge Flow-Back Over VOG

Another problem that can occur if enough electrons are present is that they can flow over the Reset Gate if the low level of the Reset clock is not set low enough. Figure 13 illustrates the effect this has on the video output. Because the sensor is being uniformly illuminated, each of the two steps (pixels) in the waveform should be approximately equal. The floating diffusion output node is saturated however, and electrons are being lost over the Reset Gate, and the second step can be seen to be less than the first step.



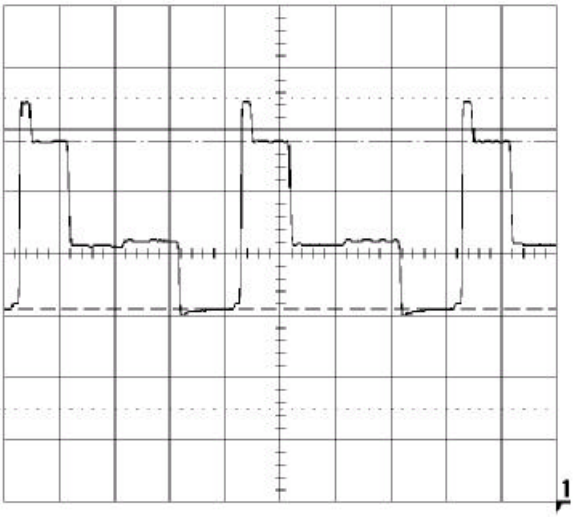


Figure 11 Charge Lost over the Reset Gate

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10.0 Lateral Overflow Drain (LOD)

Kodak's CCD Sensors fabricated with the LOD feature behave somewhat differently with respect to output saturation. The LOD serves to steer any excess charge, above that which the Vertical CCD's can handle before saturating, down the drain.

With the LOD or Anti-Blooming feature, the Vertical CCD's charge handling capacity is 30% less than a Kodak CCD Sensor without Anti-Blooming protection. However, the horizontal CCD's and the Floating Diffusion retain the same charge handling capacity.

Adjustments still need to be made to the values of VRD, VOG, and Reset Clock in order to optimize the Floating Diffusion's charge handling capacity.

11.0 Summary

To operate Kodak Full Frame CCD sensors in binning modes, adjustments must be made to the CCD clock timing, CCD bias voltages and video processing timing.

The Vertical Clocks' (V1, V2) timing must be adjusted depending on how many lines of charge are going to be transported into the Horizontal CCD register (parallel shifting of charge) before the charge is transported out of this register to the floating diffusion output node (serial shifting of the charge).

The Reset clock timing must be adjusted depending on how many pixels of charge are allowed to accumulate on the floating diffusion before being sensed by off chip electronics and then swept down the Reset Drain.

The video processing timing (CDS clocks Clamp and Sample) must be synchronized with the proper regions of the output video signal.

The CCD bias voltages VRD and VOG must be adjusted to increase the depth of the floating diffusion output node. VRD should be increased to 11.5V, and VOG should be decreased to 3V.

The Reset Clock voltage swing then must be adjusted as well, and should swing from -3V to +4V.

Note:
These operating voltages may have to be adjusted on a sensor by sensor basis for optimal performance.